University of Massachusetts Amherst

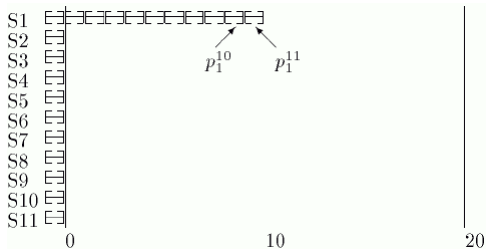
# ECE697AA – Lecture 23

## Scheduling II

Tilman Wolf
Department of Electrical and Computer Engineering
12/02/08

## Problems with WFQ

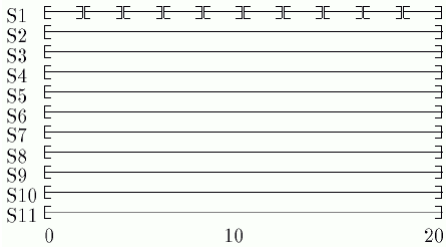
- WFQ might give "unbalanced" service
  - Large discrepancies between WFQ and GPS
  - GPS ("Generalized Processor Sharing")=bit-wise round robin
- Example scenario
  - Flow 1: 50% link bandwidth, Flows 2-11: 5% link bandwidth
  - Packet arrivals:




  - What should a good schedule look like?

# Problems with WFQ

- WFQ emulates GPS
  - GPS schedule:
    - » Flow 1 sends 10x of other flows

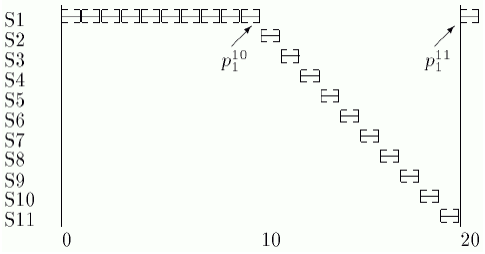



  - What are the finish times of the packets?



# Problems with WFQ

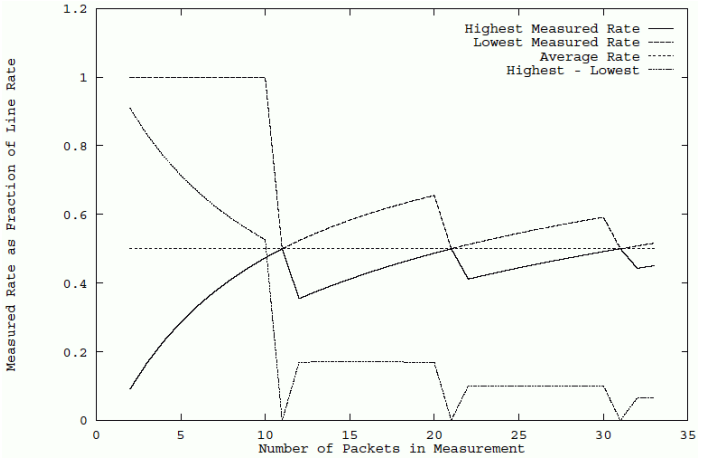
- Resulting WFQ schedule




- Problems:
  - Temporarily large differences between flows
  - Bursty schedule for Flow 1
    - » Causes bad interactions with congestion control algorithms

# Problems with WFQ

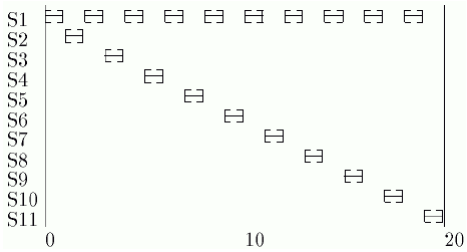
- Illustration of differences






# WF$^2$Q

- Worst-case Fair Weighted Fair Queuing (WF$^2$Q)
  - Achieves balanced scheduling



# WF²Q

- WF²Q properties
  - Bounds on differences between WF²Q and GPS

$$d^k_{i,WF^2Q} - d^k_{i,GPS} \leq \frac{L_{\max}}{r}$$

    - » Difference in departure time less than fraction of max pkt size

$$W_{i,WF^2Q}(0,r) - W_{i,GPS}(0,r) \leq L_{\max}$$

    - » Long-term difference in service is limited to max packet size

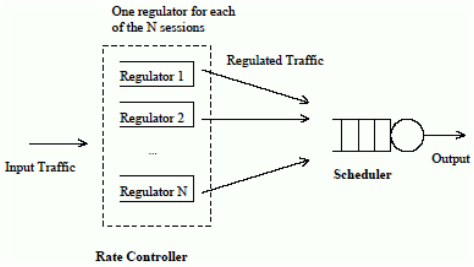
$$W_{i,GPS}(0,r) - W_{i,WF^2Q}(0,r) \leq \left(1 - \frac{r_i}{r}\right) L_{i,\max}$$

    - » "Run-ahead" of WF²Q limited to fraction of max packet size



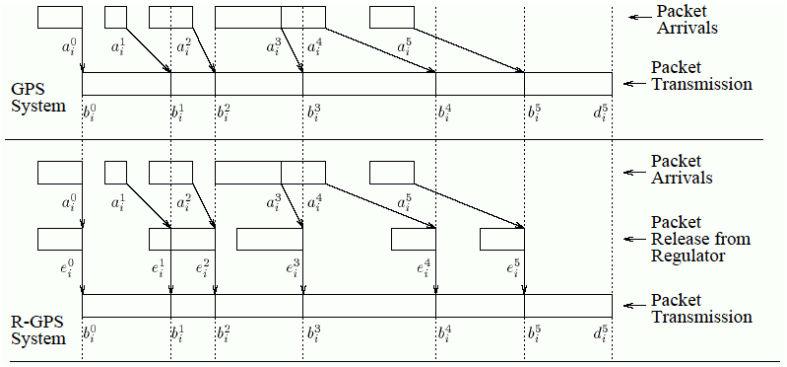
# WF²Q implementation

- Packets need to be delayed to avoid run-ahead
  - Packet should arrive at the last possible moment
- Rate-controlled service
  - Regulator delays traffic
  - Scheduler gets packets just in time
- Delay
  - Until GPS would have started the packet
- Scheduler
  - Can be WFQ



# WF$^2$Q operation

- Rate-controlled service example:




- What is the schedule of original example?

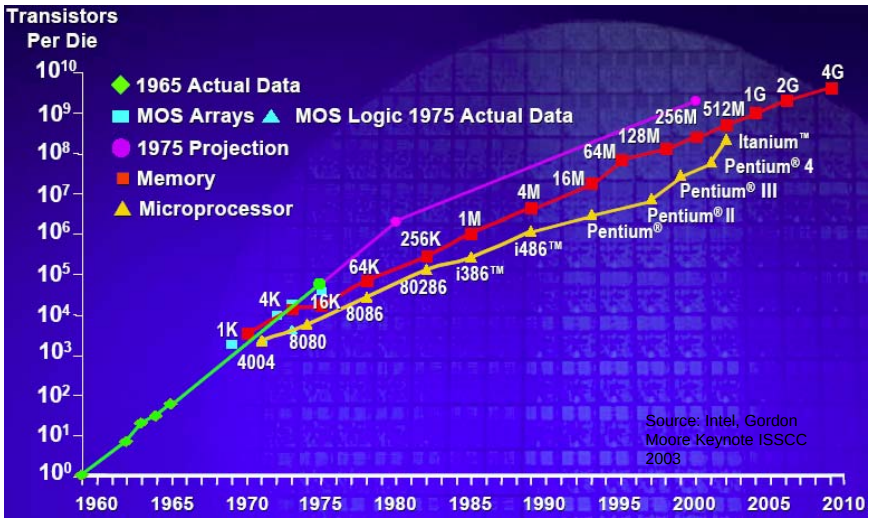


# Specialized Hardware in Routers

- Performance demands custom logic implementation
  - IP lookup in hardware
  - Flow classification in hardware
  - Scheduling in hardware
  - Cryptographic algorithms in hardware
  - String search in hardware (IDS)
- Flexibility demands programmability
  - Changing classification algorithms
  - Changing protocols
  - New control and management functions
- Tension between performance and flexibility

# Processors Increase in Performance

- Moore's law





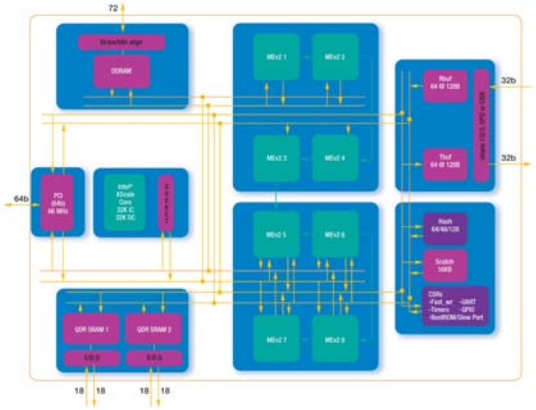

# Technology Trends

- Never underestimate Moore's law
  - Figure from original 1965 paper

# Network Processors

- Embedded multi-core processors
  - Optimized for high-performance I/O
  - Optimized for simple, highly parallel workloads
- Typical architecture



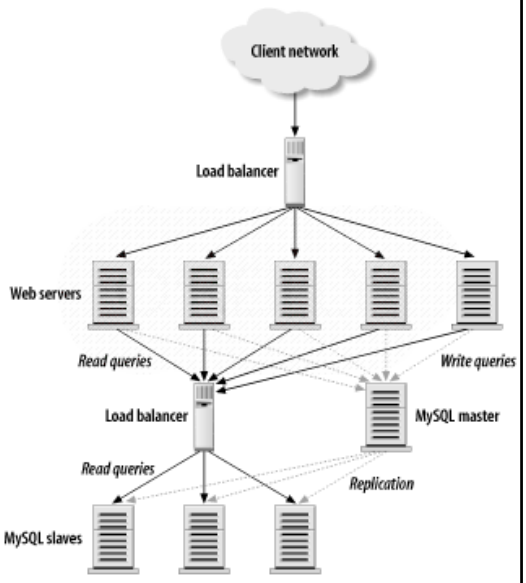



# Data Center

- Servers often end up in one place
  - Network connectivity
  - Power & cooling
  - Management

# Data Center

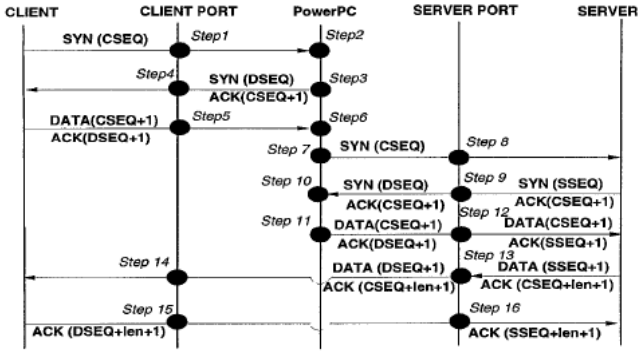
- Multi-tier architecture
  - Front end load balancer
  - Web servers
  - Back end databases
- Challenge
  - Managing connections






# Web Switching

- TCP connection needs to be established before request is known
  - G. Apostolopoulos, D. Aubespin, V. Peris, P. Pradhan, and D. Saha, "Design, Implementation and Performance of a ContentBased Switch," IEEE INFOCOM, March 2000.



# Homework

- Read
  - Anja Feldmann, “Internet clean-slate design: what and why?,” ACM SIGCOMM Computer Communication Review, vol. 37, no. 3, pp. 59–64, July 2007.
- SPARK
  - Assessment quiz